COMP 122/L Lecture 24

Kyle Dewey

Outline

- Sequential circuits
  - D flip-flops

Sequential Circuits

Motivation

```
Output = Input1 + Input2
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Combinatorial Logic

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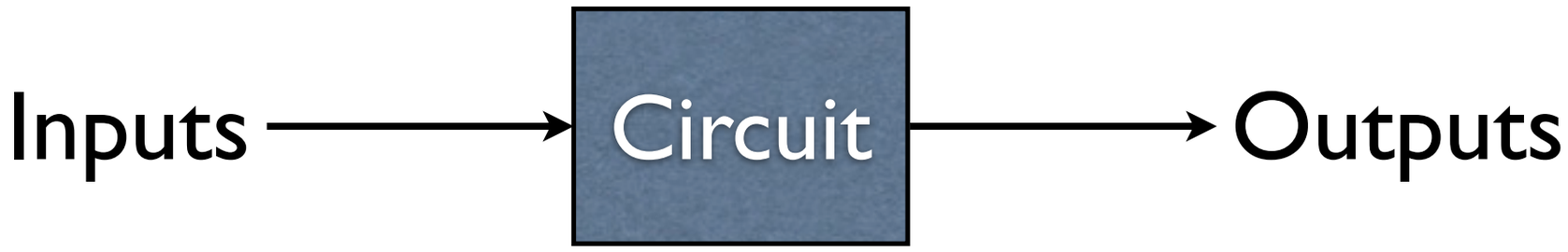
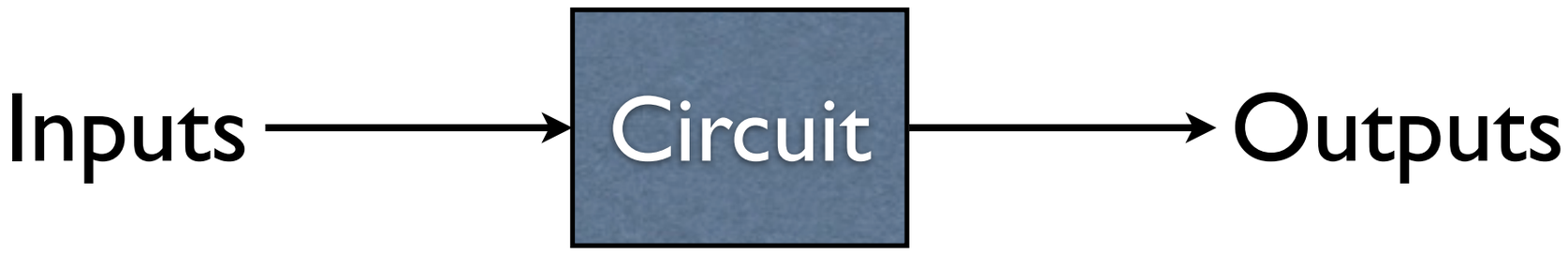
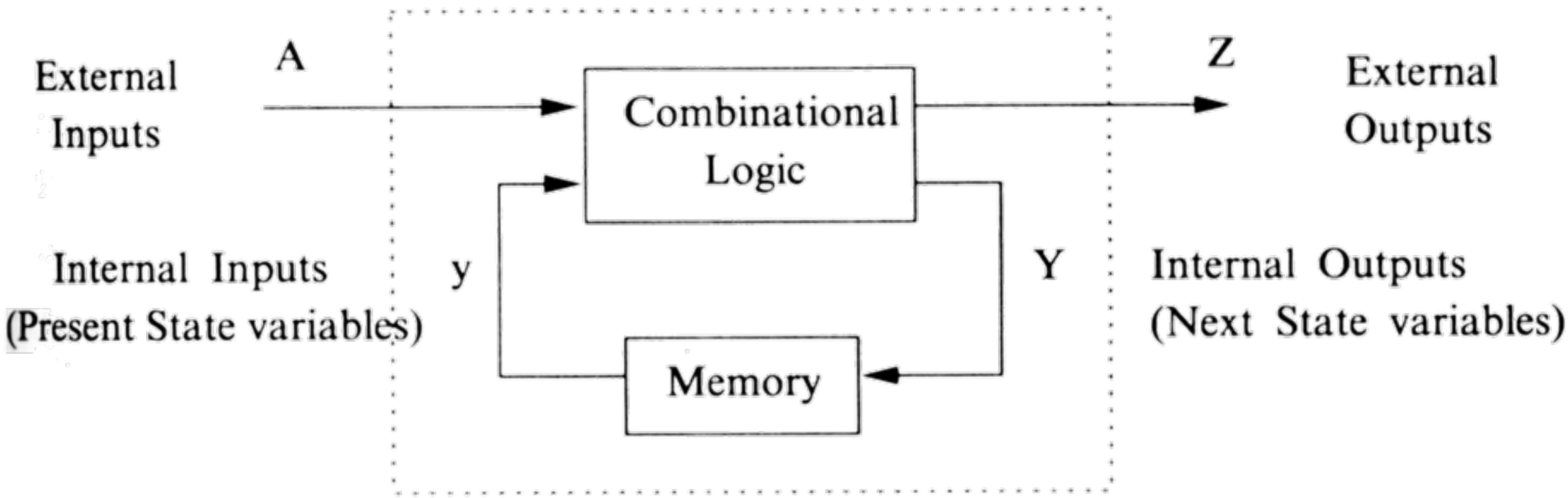


Combinatorial Logic



Sequential Logic



Saving Bits

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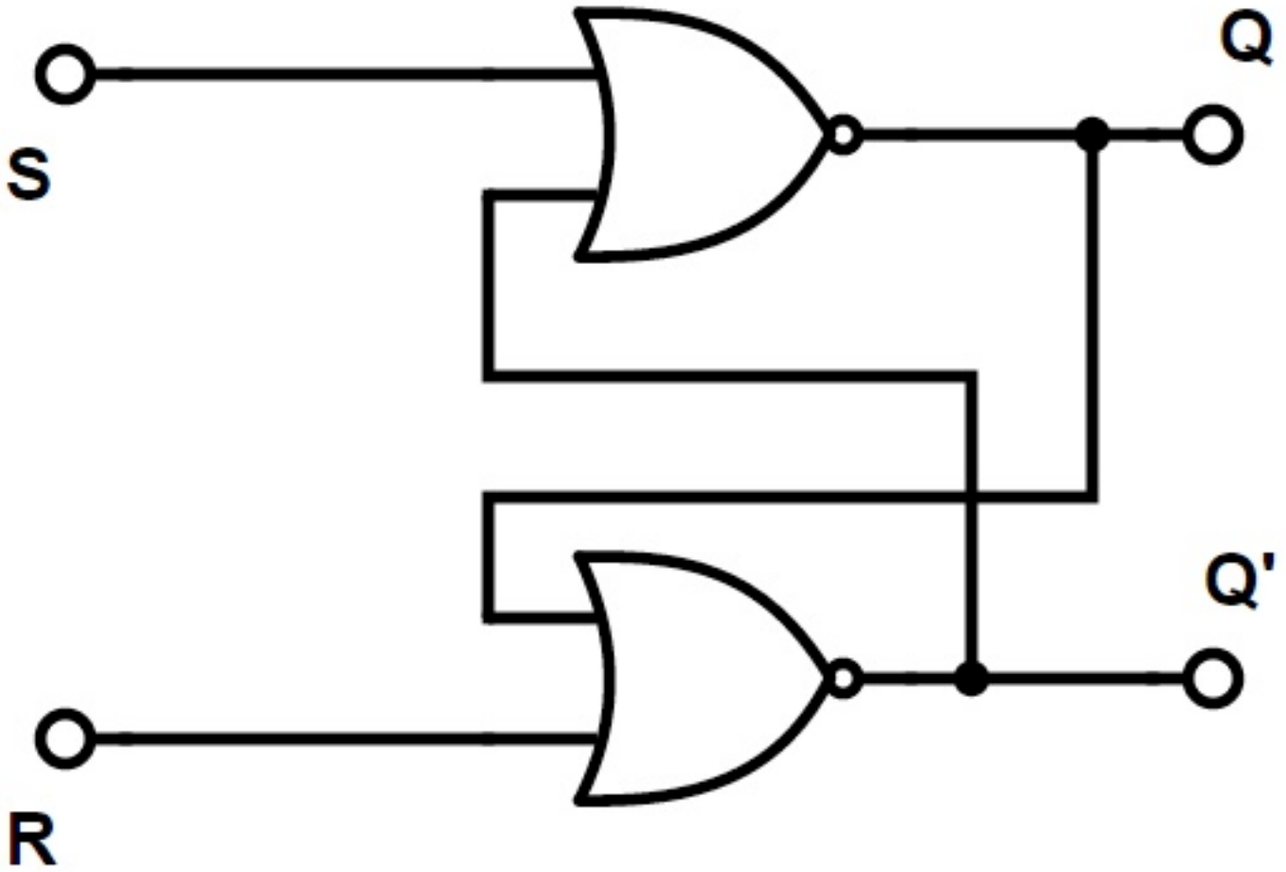

(SR Latch)

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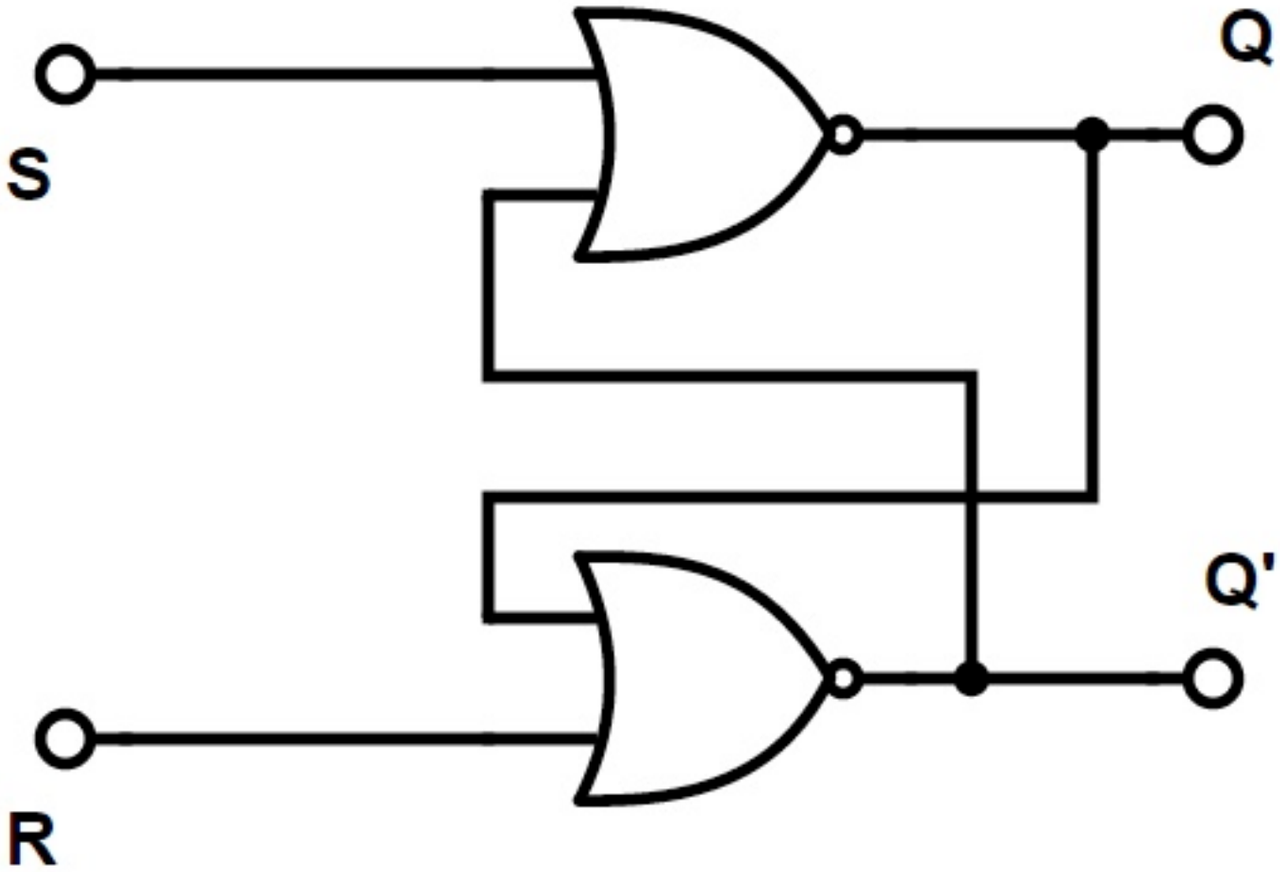

(SR Latch)

S	R	Next Q
0	0	Q
0	1	0
1	0	1
1	1	X

Building Up

Can use this to store any bit

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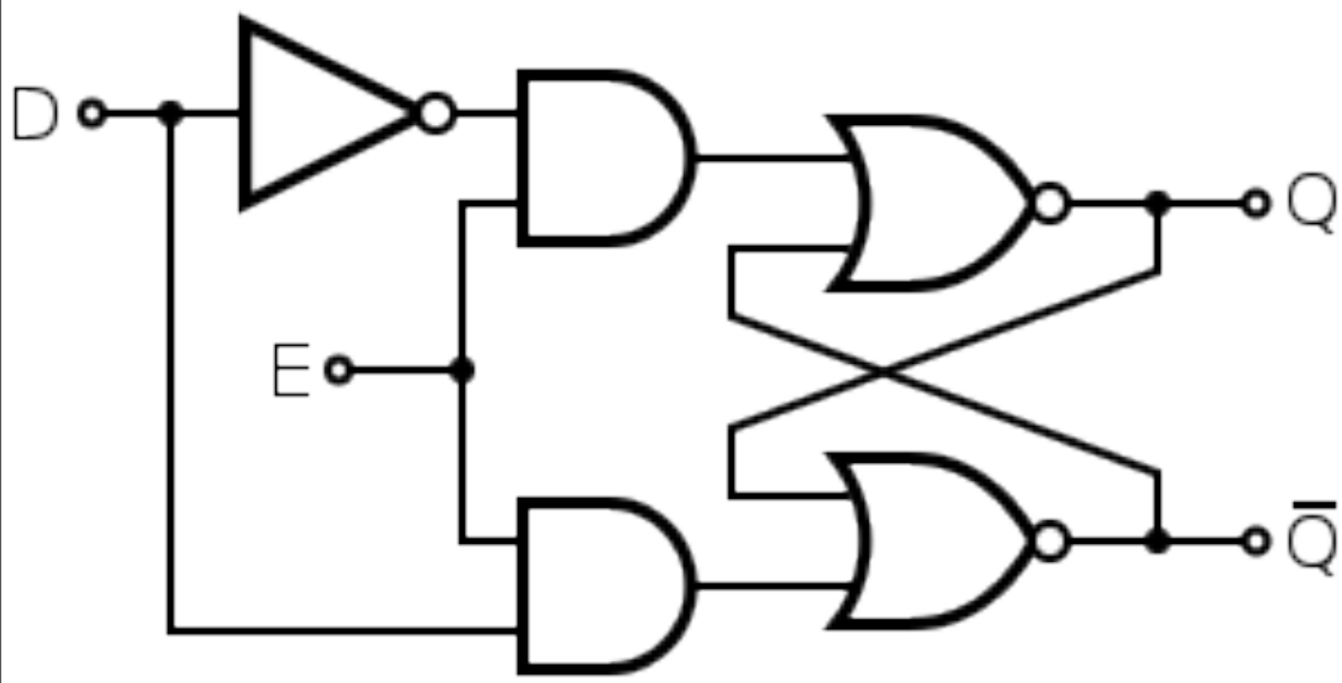

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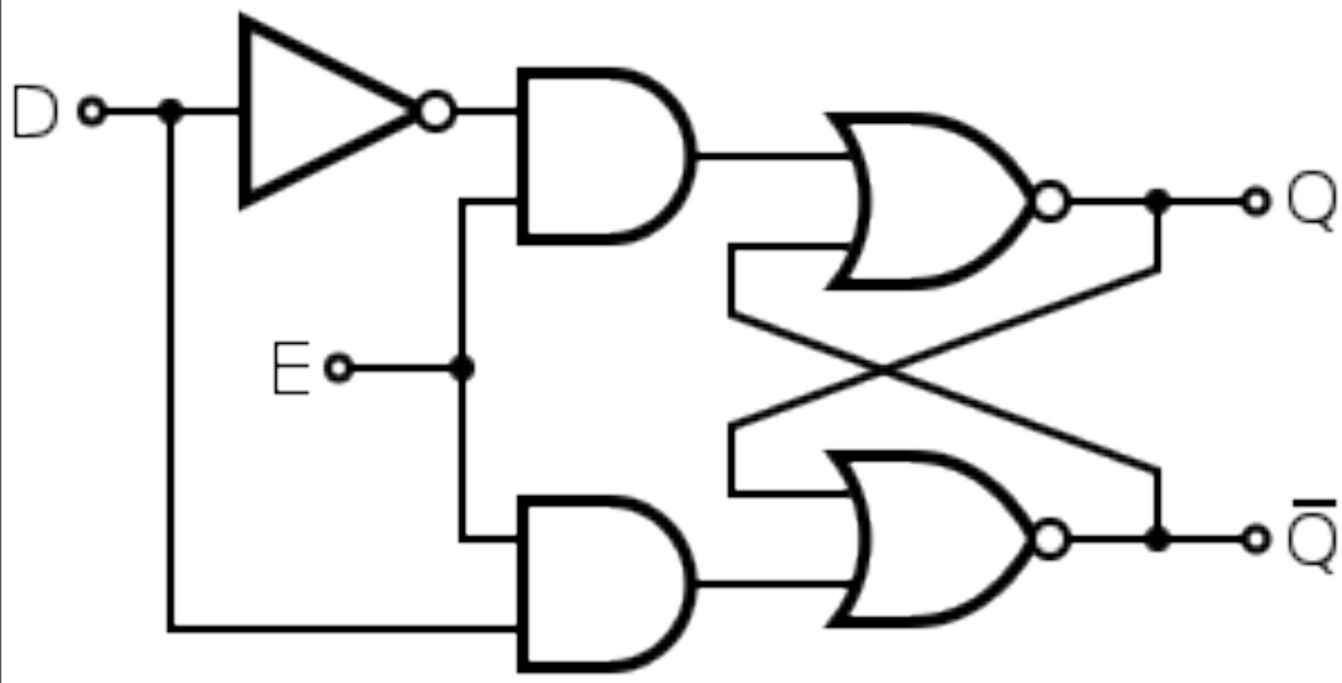

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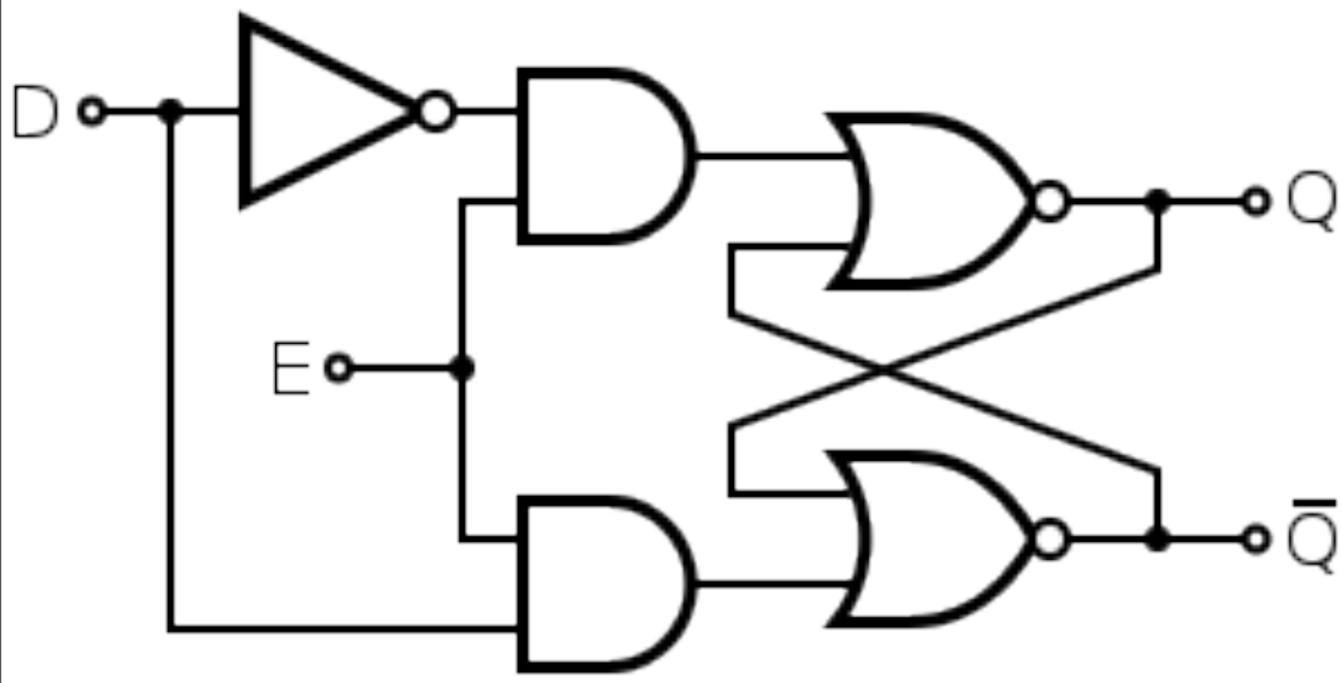
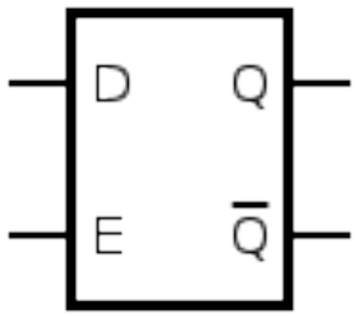


(D Latch)

Component shorthand:



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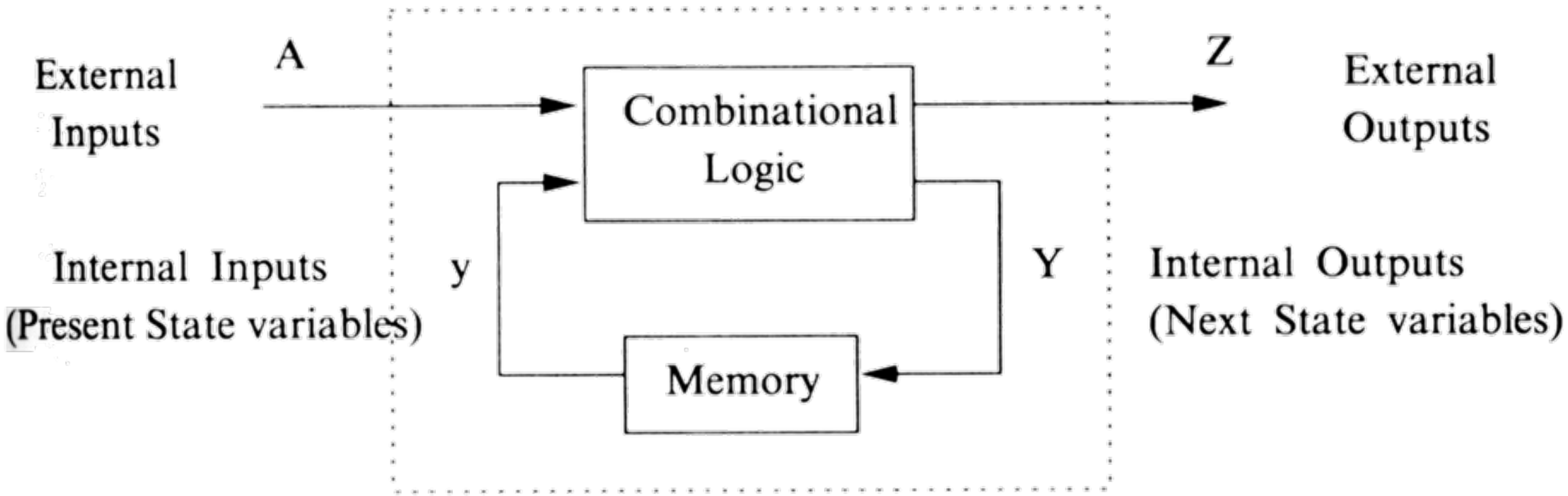
Question

How fast can this go?



Gate Delay

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Z = X!X
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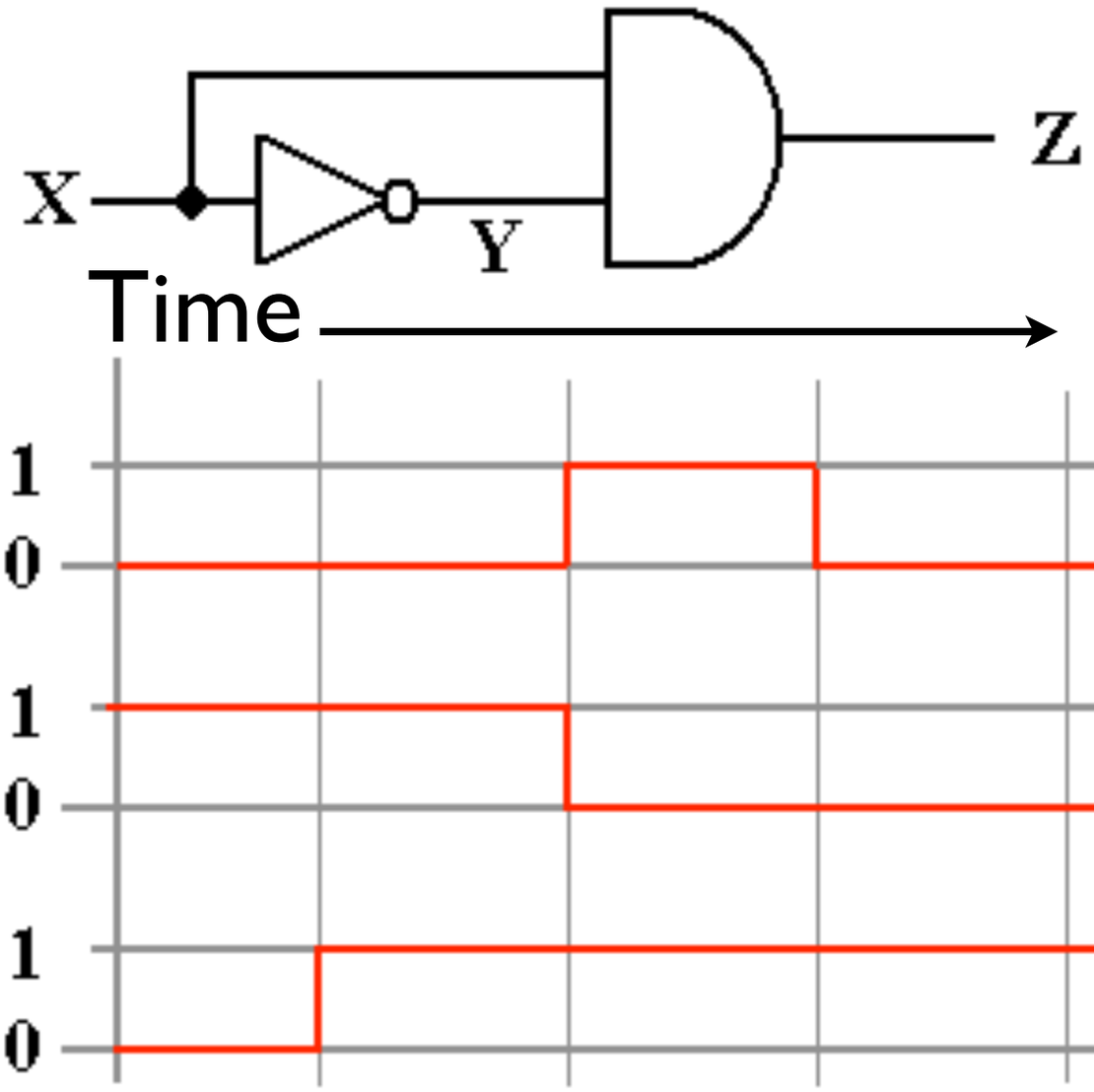

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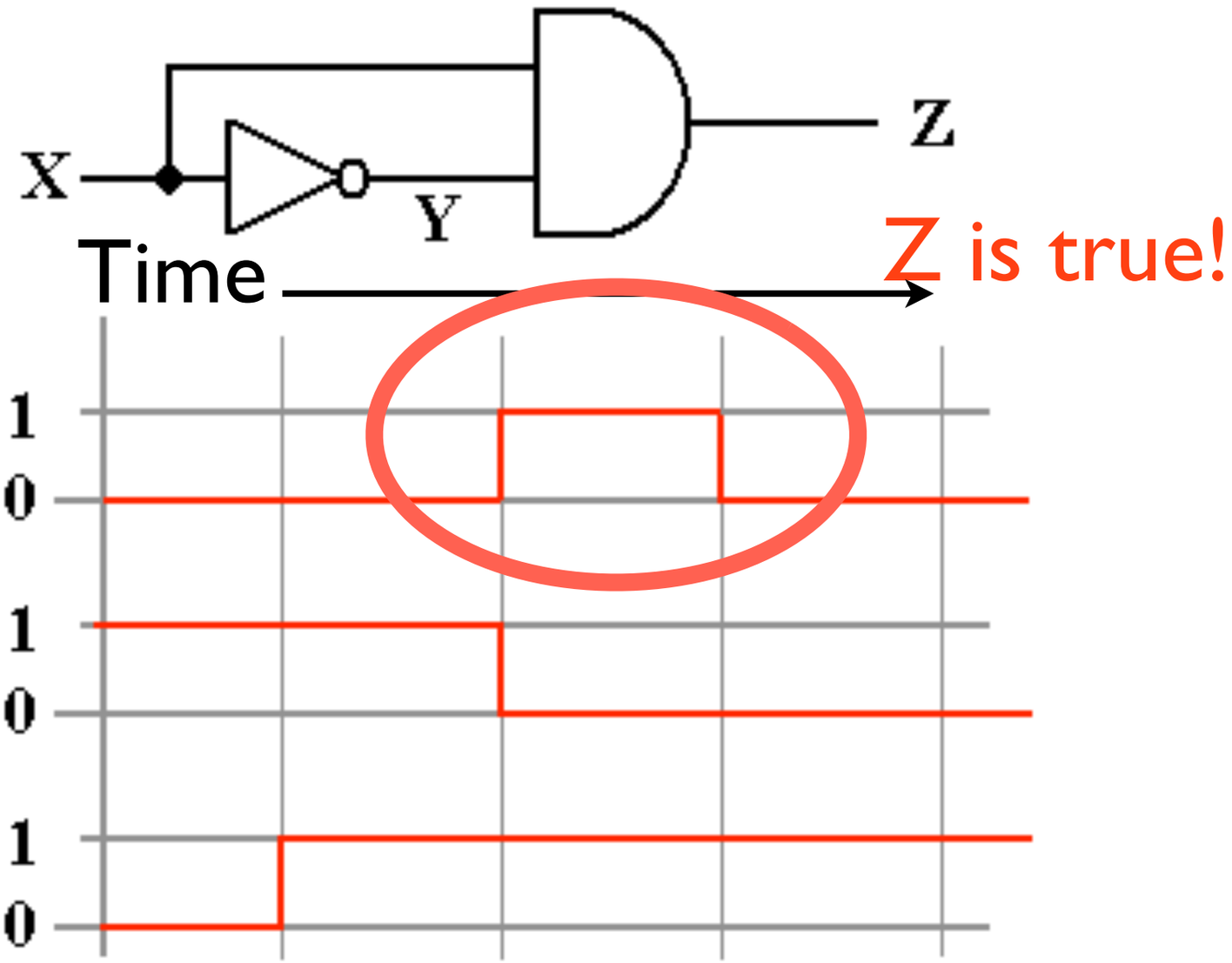
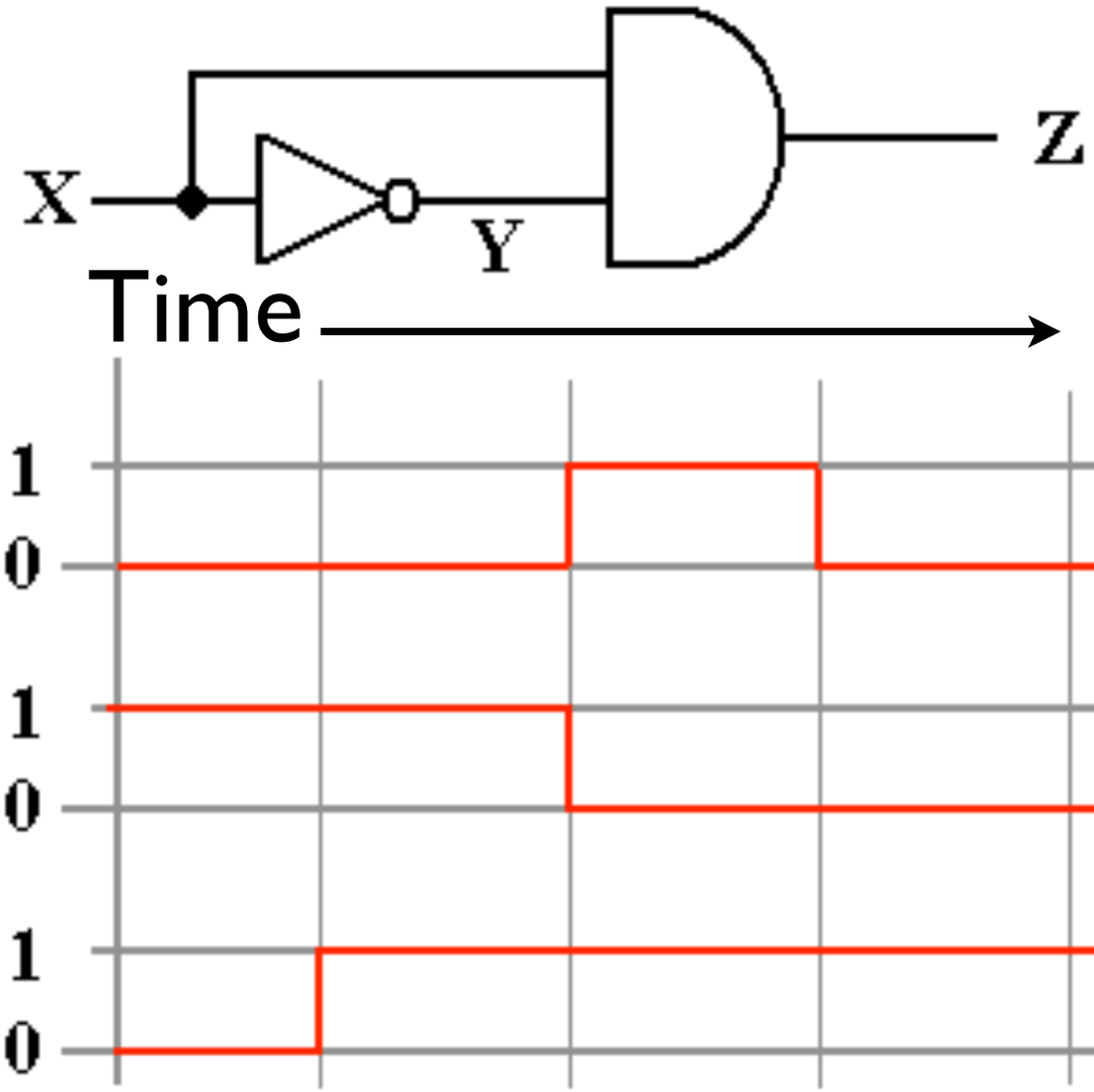


Solution

Only look at the outputs at preset intervals.

Space the intervals so the circuit will always be stable by that point.



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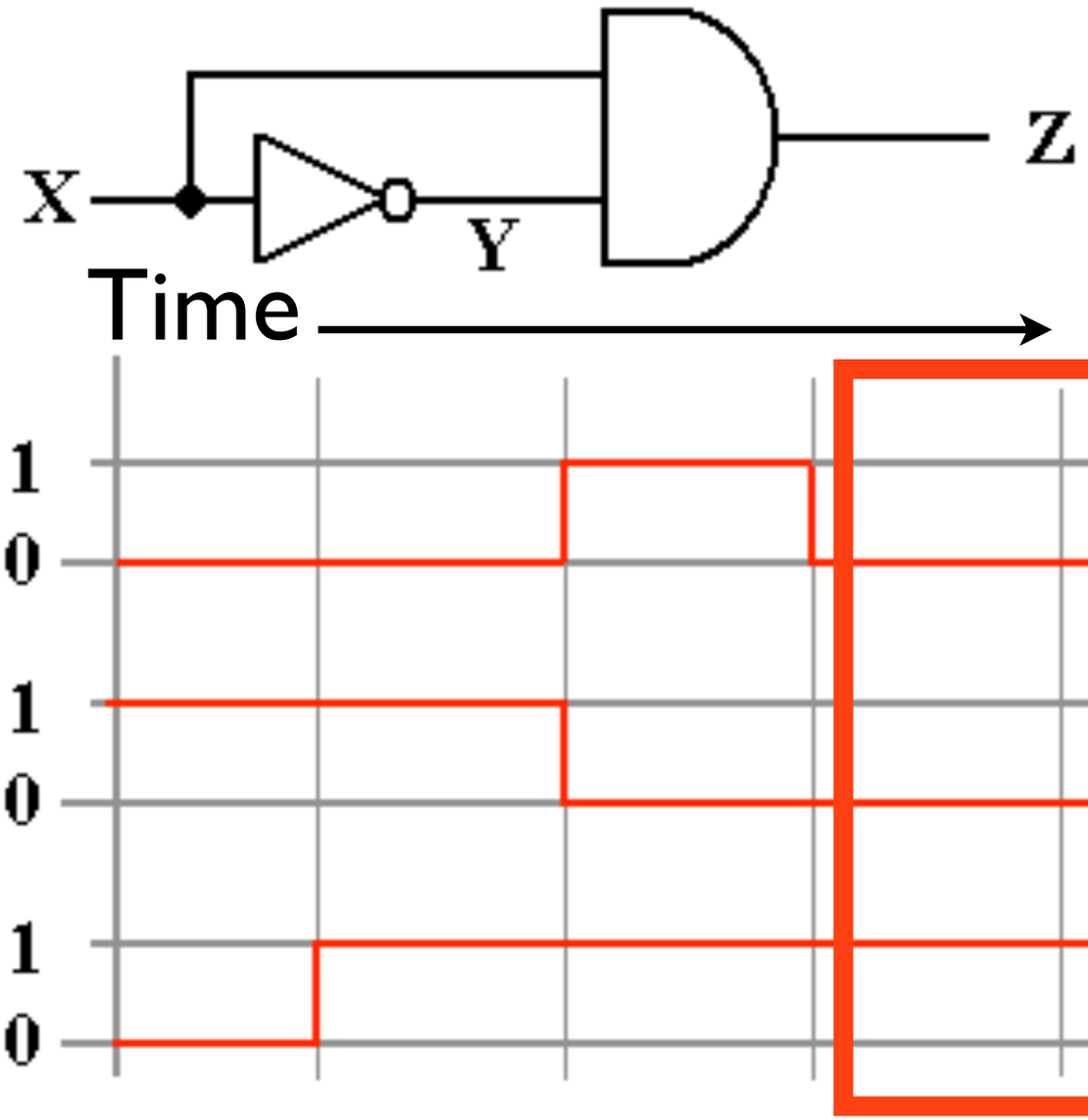

Look here
(sample here)

Intervals

Produced by a clock generator: another kind of circuit

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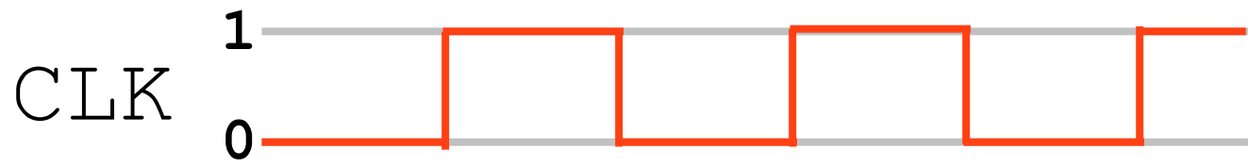

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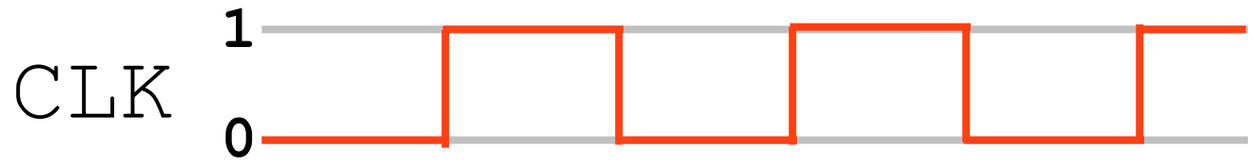

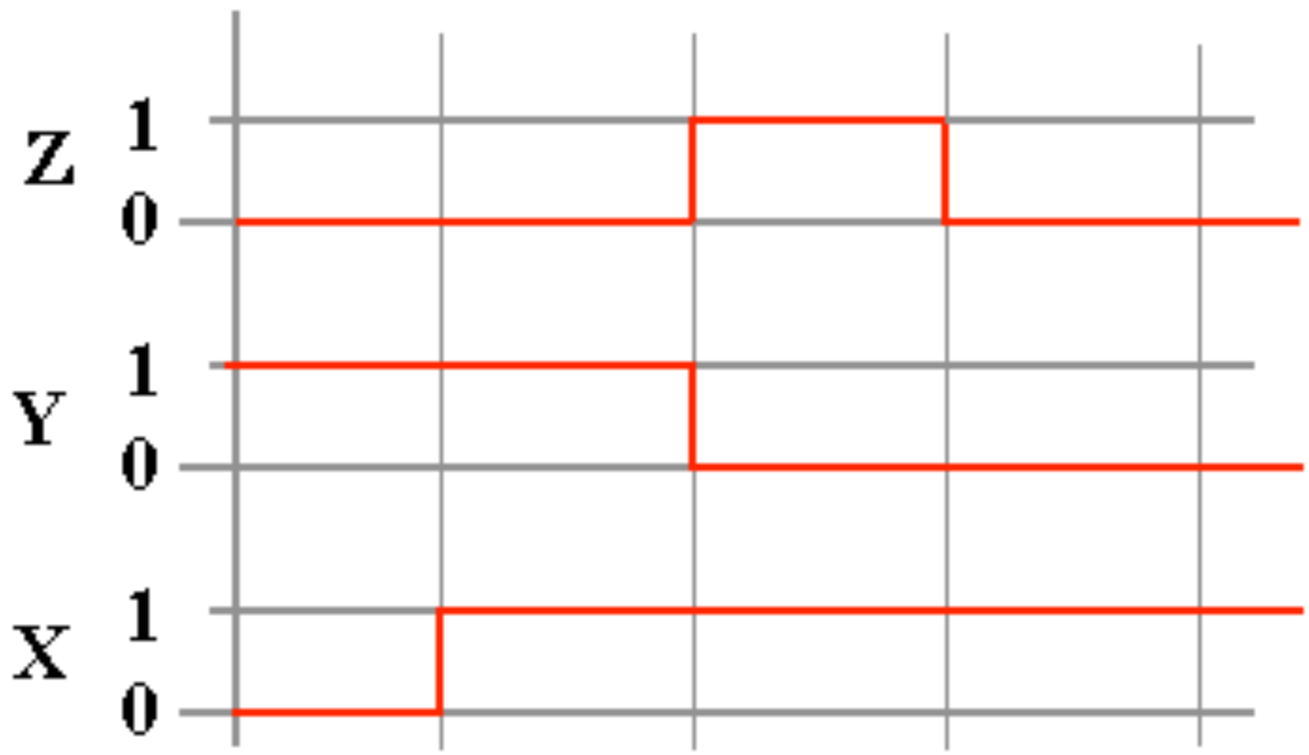

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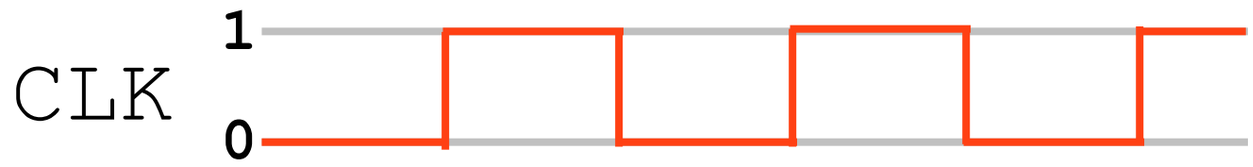

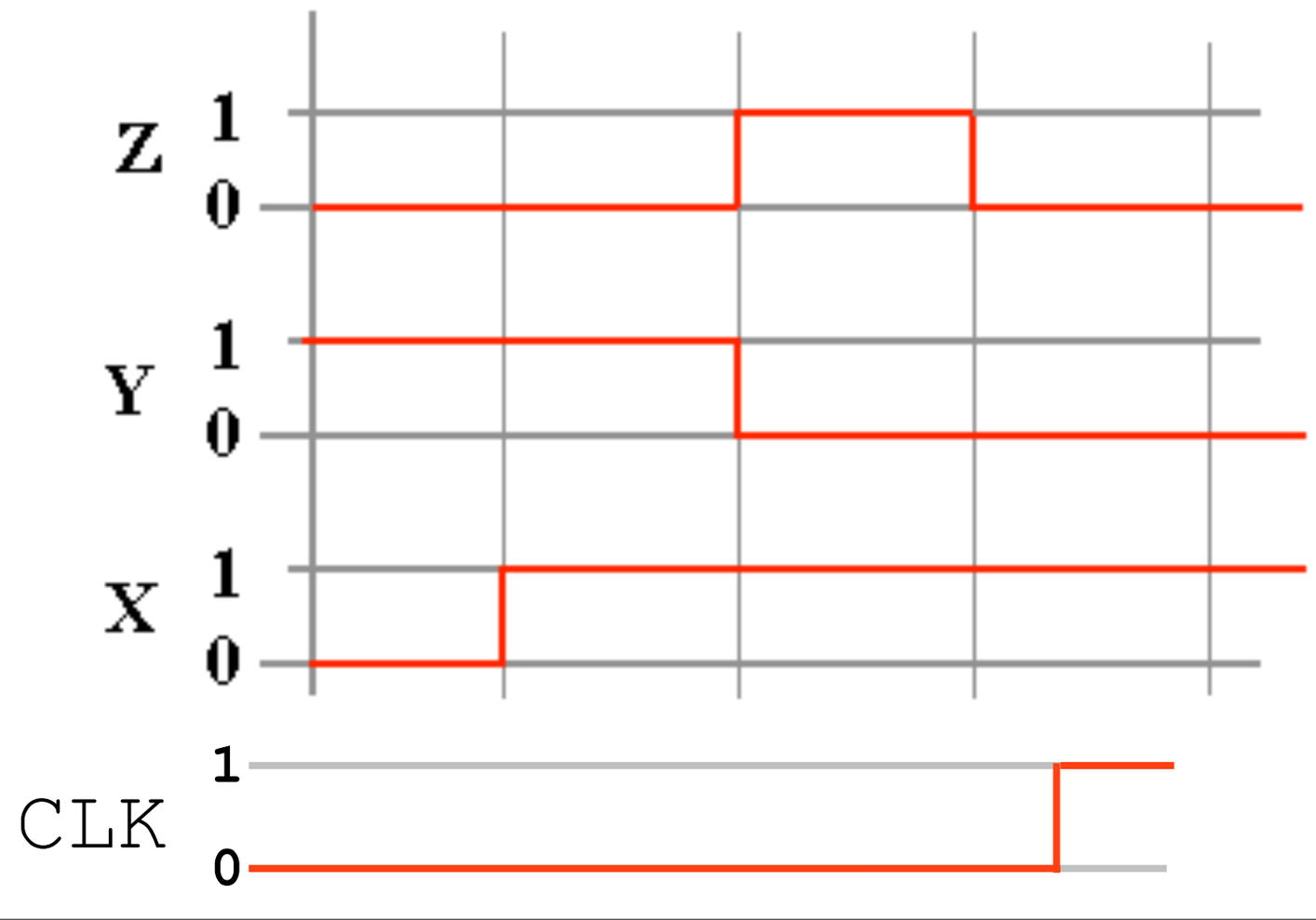

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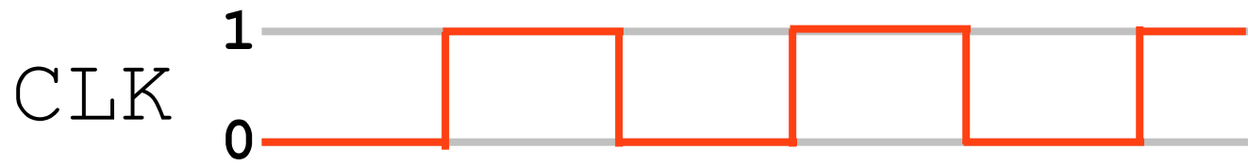
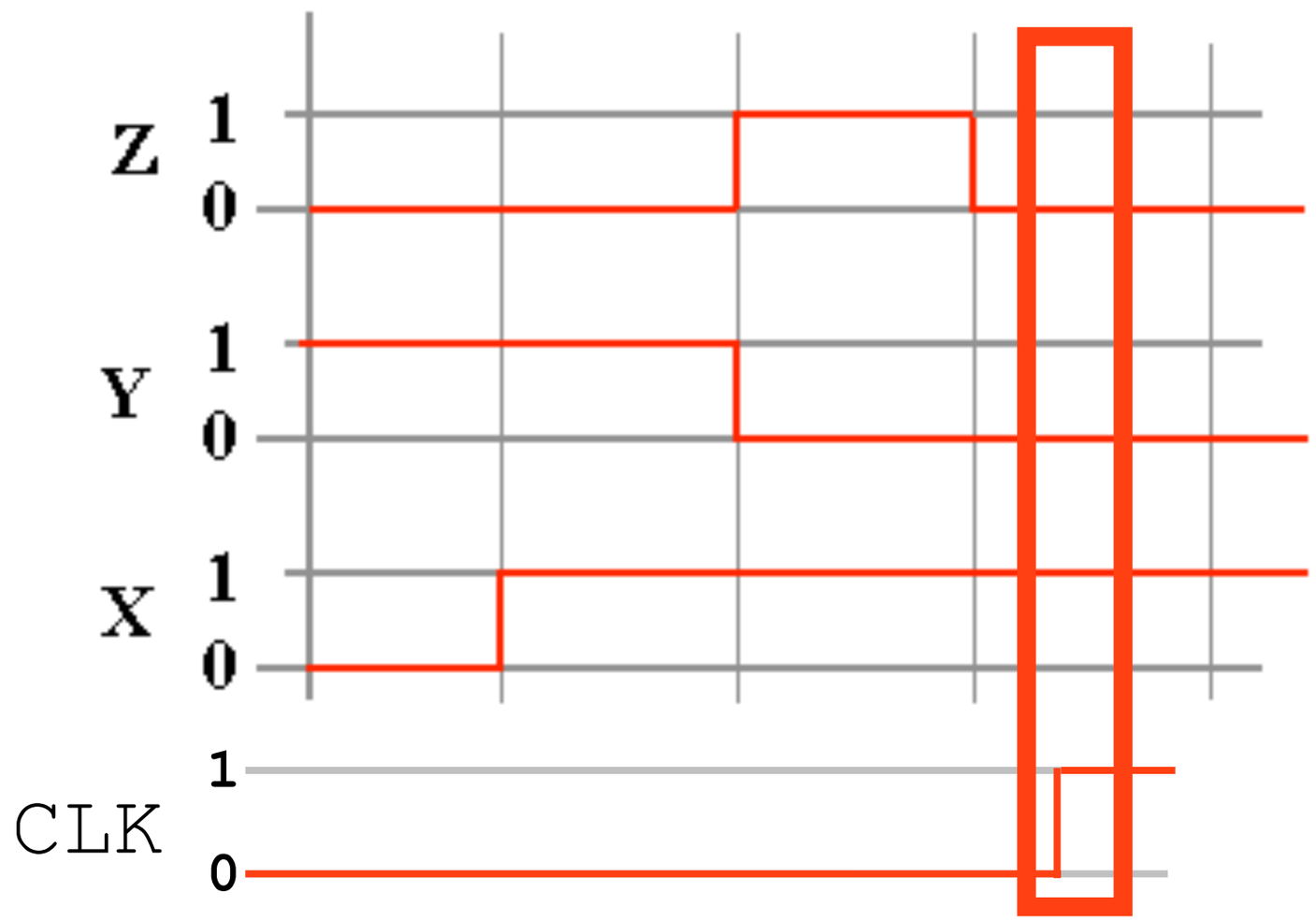
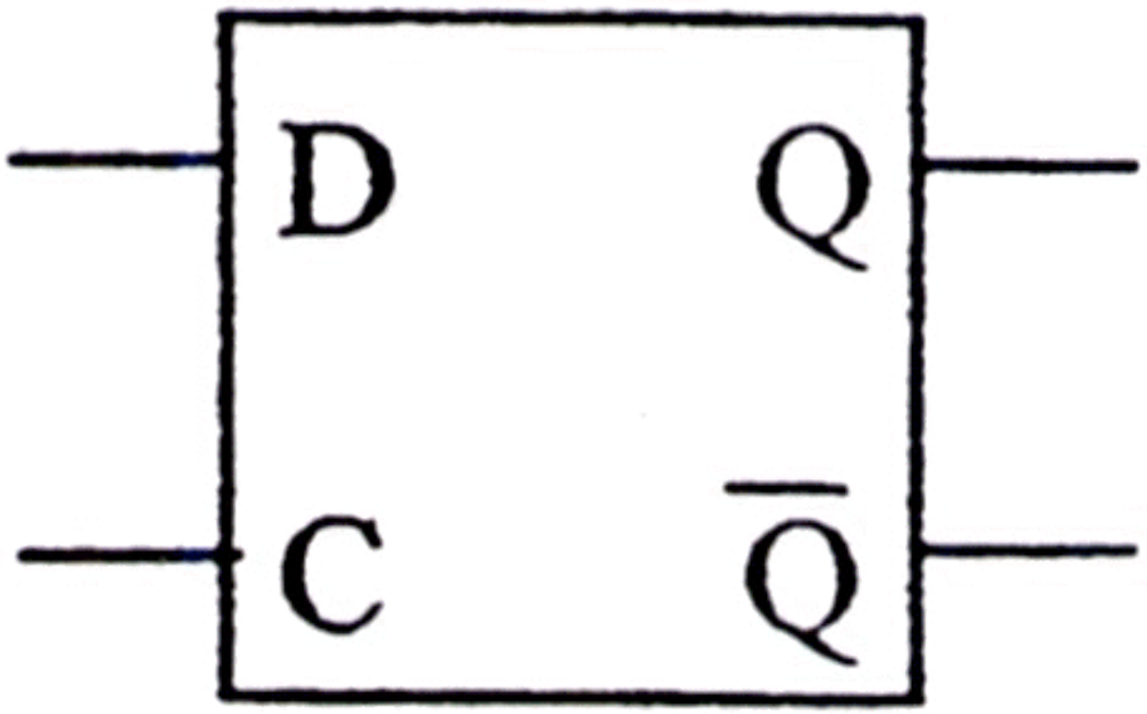




For example: sample on rising edge of clock signal

D flip-flop



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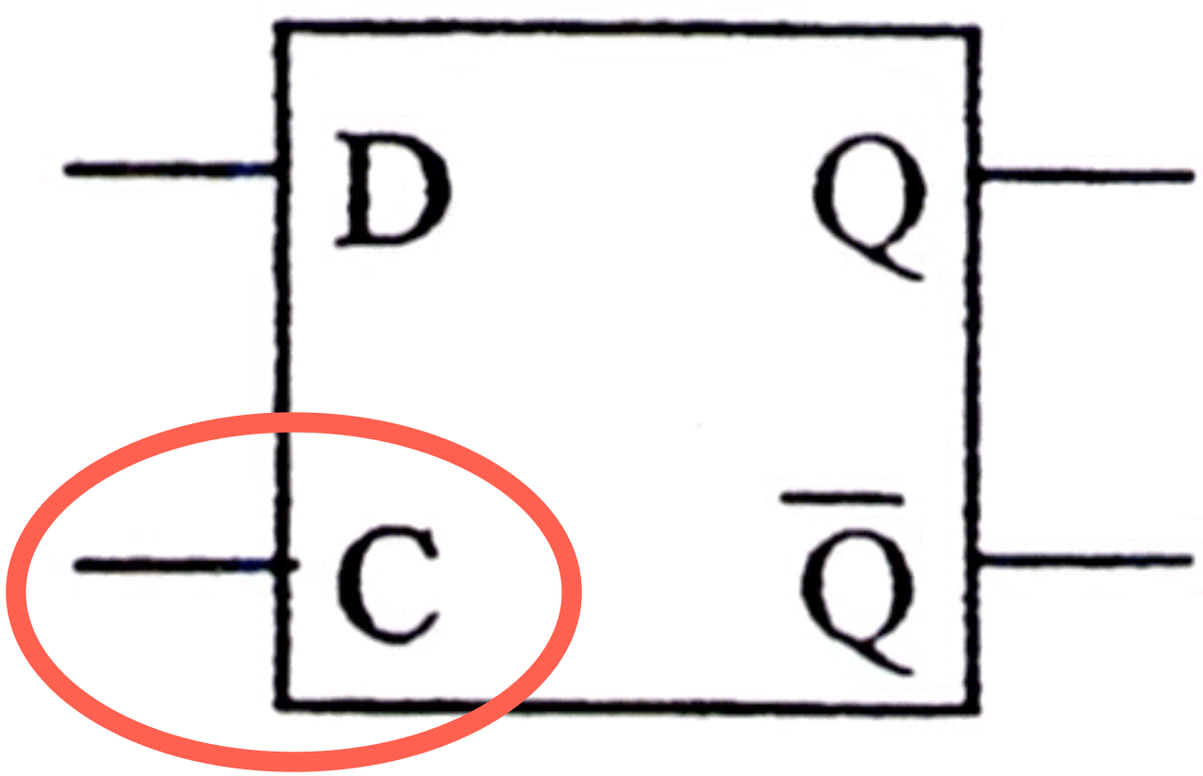

Clock input.

This could be triggered on the rising edge, depending on the component